

SPECIFICATIONS

NI 6320/6321/6323

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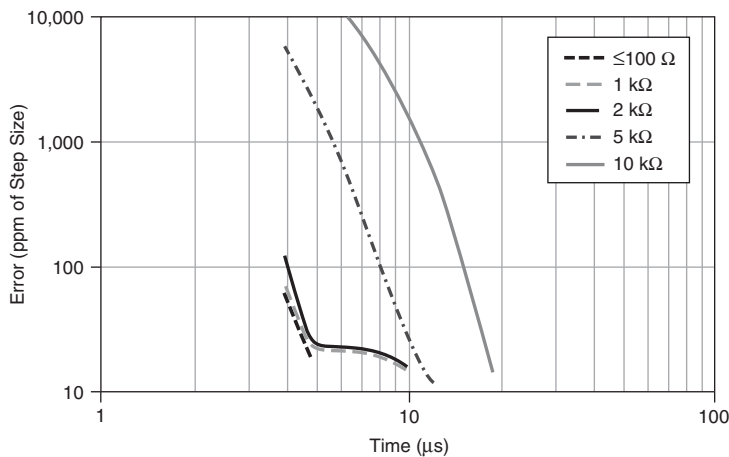
Specifications listed below are typical at 25 °C unless otherwise noted. Refer to the *X Series User Manual* for more information about NI PCIe-6320/6321/6323 devices.

Analog Input

Number of channels	
NI 6320/6321	8 differential or 16 single ended
NI 6323	16 differential or 32 single ended
ADC resolution	16 bits
DNL	No missing codes guaranteed
INL	Refer to <i>AI Absolute Accuracy</i>
Sampling rate	
Maximum	250 kS/s single channel, 250 kS/s multi-channel (aggregate)
Minimum	No minimum
Timing accuracy	50 ppm of sample rate
Timing resolution	10 ns
Input coupling	DC
Input range	± 10 V, ± 5 V, ± 1 V, ± 0.2 V
Maximum working voltage for analog inputs (signal + common mode)	± 11 V of AI GND
CMRR (DC to 60 Hz)	100 dB
Input impedance	
Device on	
AI+ to AI GND	>10 G Ω in parallel with 100 pF
AI- to AI GND	>10 G Ω in parallel with 100 pF
Device off	
AI+ to AI GND	1200 Ω
AI- to AI GND	1200 Ω

Input bias current	±100 pA
Crosstalk (at 100 kHz)	
Adjacent channels	-75 dB
Non-adjacent channels	-90 dB
Small signal bandwidth (-3 dB)	700 kHz
Input FIFO size	4,095 samples
Scan list memory	4,095 entries
Data transfers	DMA (scatter-gather), programmed I/O
Overvoltage protection (AI <0.31>, AI SENSE, AI SENSE 2)	
Device on	±25 V for up to two AI pins
Device off	±15 V for up to two AI pins
Input current during overvoltage condition	±20 mA max/AI pin
Settling time for multichannel measurements, accuracy, full scale step, all ranges	
±90 ppm of step (±6 LSB)	4 µs convert interval
±30 ppm of step (±2 LSB)	5 µs convert interval
±15 ppm of step (±1 LSB)	7 µs convert interval

Figure 1. Settling Error versus Time for Different Source Impedances



Analog triggers None

AI Absolute Accuracy

Table 1. Analog Input Absolute Accuracy

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Random Noise, σ (μ Vrms)	Absolute Accuracy at Full Scale* (μ V)
Positive Full Scale	Negative Full Scale								
10	-10	65	7.3	5	13	24	60	229	2200
5	-5	72	7.3	5	13	25	60	118	1140
1	-1	78	7.3	5	17	37	60	26	257
0.2	-0.2	105	7.3	5	27	93	60	12	69
* Refer to the <i>AI Absolute Accuracy Example</i> section.									



Note Accuracies listed are valid for up to two years from the device external calibration.

AI Absolute Accuracy Equation

Absolute Accuracy = Reading · (Gain Error) + Range · (Offset Error) + Noise Uncertainty

*Gain Error = Residual Gain Error + Gain Tempco ·
(Temp Change From Last Internal Cal) + Reference Tempco ·
(Temp Change From Last External Cal)*

*Offset Error = Residual Offset Error + Offset Tempco ·
(Temp Change From Last Internal Cal) + INL Error*

*Noise Uncertainty = $\frac{\text{Random Noise} \cdot 3}{\sqrt{10,000}}$ for a coverage factor of 3 σ and averaging
10,000 points.*

AI Absolute Accuracy Example

Absolute accuracy at full scale on the analog input channels is determined using the following assumptions:

- *Temp Change From Last External Cal = 10 °C*
- *Temp Change From Last Internal Cal = 1 °C*
- *Number of Readings = 10,000*
- *Coverage Factor = 3 σ*

For example, on the 10 V range, the absolute accuracy at full scale is as follows:

Gain Error = 65 ppm + 7.3 ppm · 1 + 5 ppm · 10 = 122 ppm

Offset Error = 13 ppm + 24 ppm · 1 + 60 ppm = 97 ppm

Noise Uncertainty = $\frac{229 \mu\text{V} \cdot 3}{\sqrt{10,000}}$ = 6.9 μV

*Absolute Accuracy = 10 V · (Gain Error) + 10 V · (Offset Error) + Noise Uncertainty =
2,200 μV*

Analog Output

Number of channels

NI 6320	0
NI 6321	2
NI 6323	4

DAC resolution 16 bits

DNL ± 1 LSB

Monotonicity 16 bit guaranteed

Maximum update rate

1 channel	900 kS/s
2 channels	840 kS/s per channel

3 channels	775 kS/s per channel
4 channels	719 kS/s per channel
Timing accuracy	50 ppm of sample rate
Timing resolution.....	10 ns
Output range	±10 V
Output coupling	DC
Output impedance.....	0.2 Ω
Output current drive.....	±5 mA
Overdrive protection.....	±15 V
Overdrive current.....	15 mA
Power-on state	±20 mV
Power-on/off glitch.....	2 V for 500 ms
Output FIFO size	8,191 samples shared among channels used
Data transfers	DMA (scatter-gather), programmed I/O
AO waveform modes.....	Non-periodic waveform, periodic waveform regeneration mode from onboard FIFO, periodic waveform regeneration from host buffer including dynamic update
Settling time, full scale step, 15 ppm (1 LSB)	6 μ s
Slew rate	15 V/ μ s
Glitch energy	
Magnitude.....	100 mV
Duration	2.6 μ s

AO Absolute Accuracy

Absolute accuracy at full scale numbers is valid immediately following self calibration and assumes the device is operating within 10 °C of the last external calibration.

Nominal Range		Residual Gain Error (ppm of Reading)	Gain Tempco (ppm/°C)	Reference Tempco (ppm/°C)	Residual Offset Error (ppm of Range)	Offset Tempco (ppm of Range/°C)	INL Error (ppm of Range)	Absolute Accuracy at Full Scale* (µV)
Positive Full Scale	Negative Full Scale							
10	-10	80	11.3	5	53	4.8	128	3,271
* Refer to the <i>AO Absolute Accuracy Equation</i> section.								



Note Accuracies listed are valid for up to two years from the device external calibration.

AO Absolute Accuracy Equation

Absolute Accuracy = Output Value · (Gain Error) + Range · (Offset Error)

Gain Error = Residual Gain Error + Gain Tempco · (Temp Change From Last Internal Cal) + Reference Tempco · (Temp Change From Last External Cal)

Offset Error = Residual Offset Error + Offset Tempco · (Temp Change From Last Internal Cal) + INL Error

Static Characteristics

Number of channels	
NI 6320/6321	24 total, 8 (P0.<0..7>) 16 (PFI <0..7>/P1, PFI <8..15>/P2)
NI 6323	48 total, 32 (P0.<0..31>) 16 (PFI <0..7>/P1, PFI <8..15>/P2)
Ground reference	D GND
Direction control	Each terminal individually programmable as input or output
Pull-down resistor	50 kΩ typical, 20 kΩ minimum
Input voltage protection ¹	±20 V on up to two pins

Waveform Characteristics (Port 0 Only)

Terminals used	
NI 6320/6321	Port 0 (P0.<0..7>)
NI 6323	Port 0 (P0.<0..31>)
Port/sample size	
NI 6320/6321	Up to 8 bits
NI 6323	Up to 32 bits
Waveform generation (DO) FIFO	2,047 samples
Waveform acquisition (DI) FIFO	255 samples
DO or DI Sample Clock frequency	0 to 1 MHz, system and bus activity dependent
Data transfers	DMA (scatter-gather), programmed I/O
Digital line filter settings	160 ns, 10.24 μs, 5.12 ms, disable

PFI/Port 1/Port 2 Functionality

Functionality	Static digital input, static digital output, timing input, timing output
Timing output sources	Many AI, AO, counter, DI, DO timing signals
Debounce filter settings	90 ns, 5.12 μs, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input

¹ Stresses beyond those listed under *Input voltage protection* may cause permanent damage to the device.

Table 2. Recommended Operation Conditions

Input Voltage Level	Minimum	Maximum
Input high voltage (V_{IH})	2.2 V	5.25 V
Input low voltage (V_{IL})	0 V	0.8 V

Output high current (I_{OH})

P0.<0..31>.....-24 mA maximum
PFI <0..15>/P1/P2.....-16 mA maximum

Output low current (I_{OL})

P0.<0..31>..... 16 mA maximum
PFI <0..15>/P1/P2..... 24 mA maximum

Digital logic levels

Positive-going threshold (V_{T+}).....2.2 V maximum
Negative-going threshold (V_{T-}).....0.8 V minimum

Electrical and digital I/O characteristics

Delta VT hysteresis ($V_{T+} - V_{T-}$) 0.2 V minimum
 I_{IL} input low current ($V_{IN} = 0$ V)-10 μ A maximum
 I_{IH} input high current ($V_{IN} = 5$ V) 250 μ A maximum

Figure 2. P0.<0..31>: I_{OH} versus V_{OH}

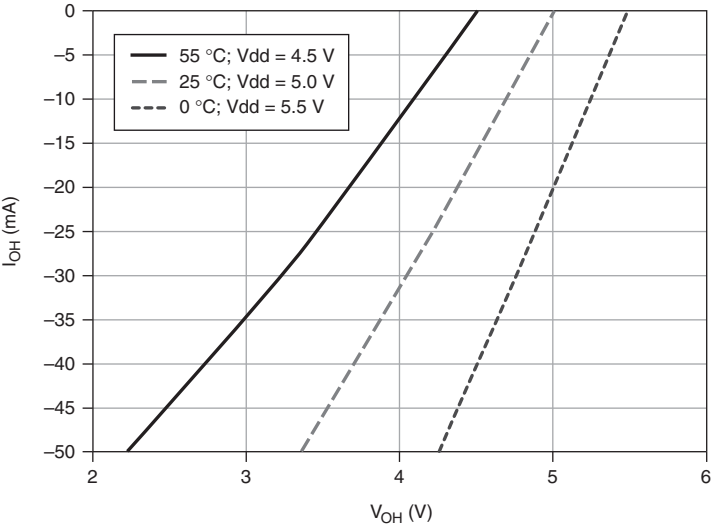


Figure 3. P0.<0..31>: I_{OL} versus V_{OL}

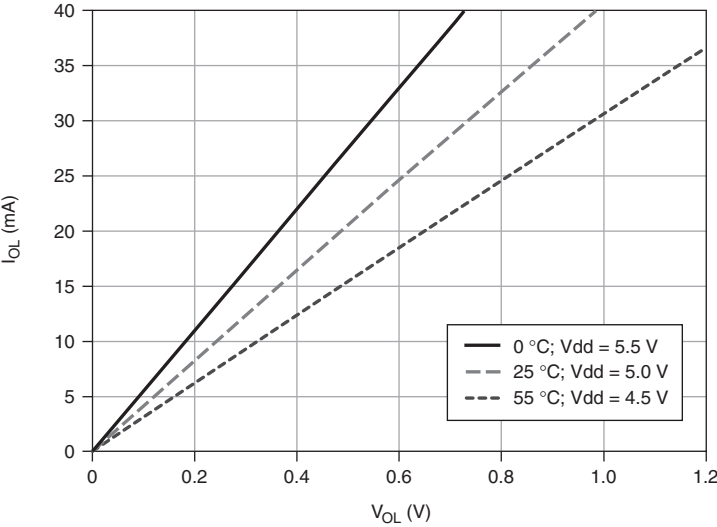


Figure 4. PFI <0..15>/P1/P2: I_{OH} versus V_{OH}

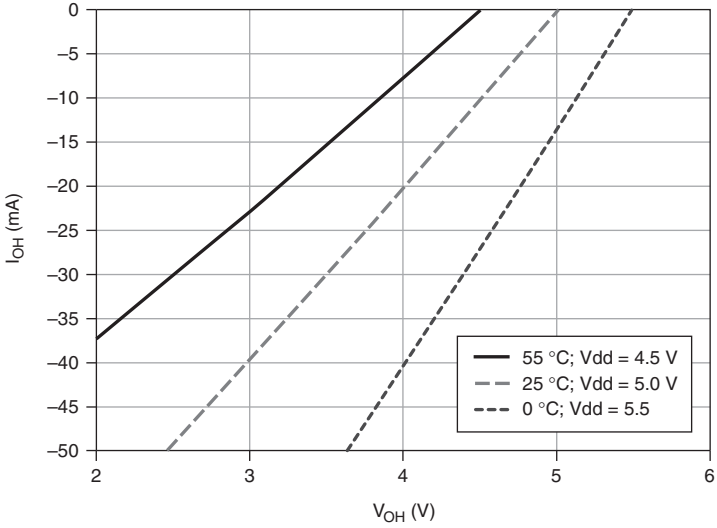
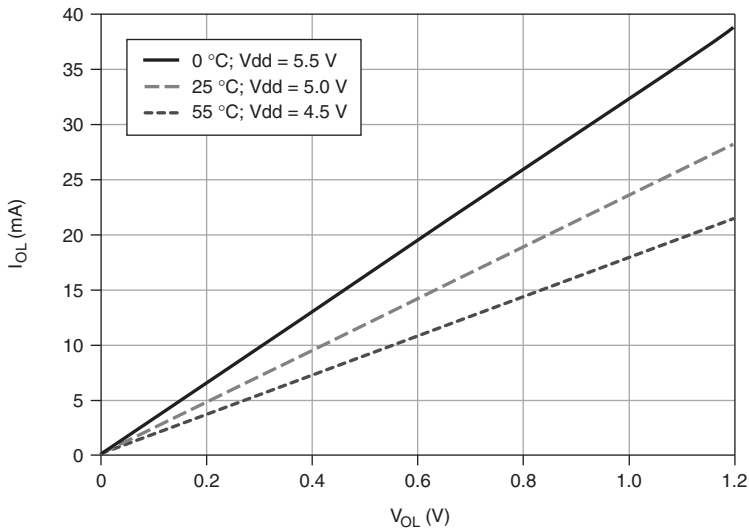


Figure 5. PFI <0..15>/P1/P2: I_{OL} versus V_{OL}



General-Purpose Counter/Timers

Number of counter/timers	4
Resolution	32 bits
Counter measurements	Edge counting, pulse, pulse width, semi-period, period, two-edge separation
Position measurements	X1, X2, X4 quadrature encoding with Channel Z reloading; two-pulse encoding
Output applications	Pulse, pulse train with dynamic updates, frequency division, equivalent time sampling
Internal base clocks	100 MHz, 20 MHz, 100 kHz
External base clock frequency	0 to 25 MHz
Base clock accuracy	50 ppm
Inputs	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Routing options for inputs	Any PFI, RTSI, many internal signals
FIFO	127 samples per counter
Data transfers	Dedicated scatter-gather DMA controller for each counter/timer, programmed I/O

Frequency Generator

Number of channels	1
Base clocks	20 MHz, 10 MHz, 100 kHz
Divisors	1 to 16
Base clock accuracy	50 ppm
Output can be available on any PFI or RTSI terminal.	

Phase-Locked Loop (PLL)

Number of PLLs	1
Reference clock locking frequencies	
RTSI <0..7>	10 MHz, 20 MHz
PFI <0..15>	10 MHz, 20 MHz
Output of PLL	100 MHz Timebase; other signals derived from 100 MHz Timebase including 20 MHz and 100 kHz Timebases

External Digital Triggers

Source	Any PFI, RTSI
Polarity	Software-selectable for most signals
Analog input function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Convert Clock, Sample Clock Timebase
Analog output function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Counter/timer functions	Gate, Source, HW_Arm, Aux, A, B, Z, Up_Down, Sample Clock
Digital waveform generation (DO) function	Start Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase
Digital waveform acquisition (DI) function	Start Trigger, Reference Trigger, Pause Trigger, Sample Clock, Sample Clock Timebase

Device-To-Device Trigger Bus

Input source	RTSI <0..7>
Output destination	RTSI <0..7>
Output selections	10 MHz Clock, frequency generator output, many internal signals

Debounce filter settings	90 ns, 5.12 μ s, 2.56 ms, custom interval, disable; programmable high and low transitions; selectable per input
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Bus Interface

Form factor	x1 PCI Express, specification v1.1 compliant
Slot compatibility	x1, x4, x8, and x16 PCI Express slots ¹
DMA channels	8, analog input, analog output, digital input, digital output, counter/timer 0, counter/timer 1, counter/timer 2, counter/timer 3

Power Requirements

Without disk drive power connector installed	
+3.3 V	1.4 W
+12 V	8.6 W
With disk drive power connector installed	
+3.3 V	1.4 W
+12 V	3 W
+5 V	15 W

Current Limits



Caution Exceeding the current limits may cause unpredictable behavior by the device and/or PC.

Without disk drive power connector installed	
P0/PFI/P1/P2 and +5 V terminals combined	1 A max
With disk drive power connector installed	
+5 V terminal (connector 0).....	1 A max ²
+5 V terminal (connector 1).....	1 A max ²
P0/PFI/P1/P2 combined	1 A max

¹ Some motherboards reserve the x16 slot for graphics use. For PCI Express guidelines, refer to ni.com/pciexpress.
² Has a self-resetting fuse that opens when current exceeds this specification.

Calibration

Recommended warm-up time..... 15 minutes
Calibration interval..... 2 years

Physical Requirements

Printed circuit board dimensions 9.9 × 16.8 cm (3.9 × 6.6 in.) (half-length)

Weight

NI 6320/6321 104 g (3.6 oz)
NI 6323 114 g (4.0 oz)

I/O connector

NI 6320/6321 1 68-pin VHDCI
NI 6323 2 68-pin VHDCI

Table 3. Mating Connectors

Manufacturer, Part Number	Description
MOLEX 71430-0011	68-Pos Right Angle Single Stack PCB-Mount VHDCI (Receptacle)
MOLEX 74337-0016	68-Pos Right Angle Dual Stack PCB-Mount VHDCI (Receptacle)
MOLEX 71425-3001	68-Pos Offset IDC Cable Connector (Plug) (SHC68-*)

Disk drive power connector..... Standard ATX peripheral connector
(not serial ATA)

Clean the hardware with a soft, nonmetallic brush.

Maximum Working Voltage¹

 **Caution** The protection provided by the DAQ device can be impaired if it is used in a manner not described in the *X Series User Manual*.

Channel to earth..... 11 V, Measurement Category I

 **Note** Measurement Categories CAT I and CAT O (Other) are equivalent. These test and measurement circuits are not intended for direct connection to the MAINS building installations of Measurement Categories CAT II, CAT III, or CAT IV.

¹ *Maximum working voltage* refers to the signal voltage plus the common-mode voltage.

Environmental

Operating temperature	0 to 50 °C
Storage temperature	-40 to 70 °C
Operating humidity	10 to 90% RH, noncondensing
Storage humidity	5 to 95% RH, noncondensing
Pollution Degree	2
Maximum altitude	2,000 m
Indoor use only.	

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the [Online Product Certification](#) section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.



Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.



Note For EMC declarations and certifications, and additional information, refer to the [Online Product Certification](#) section.

CE Compliance C €

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity (DoC) for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

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Figure 6. NI PCIe-6320 Pinout

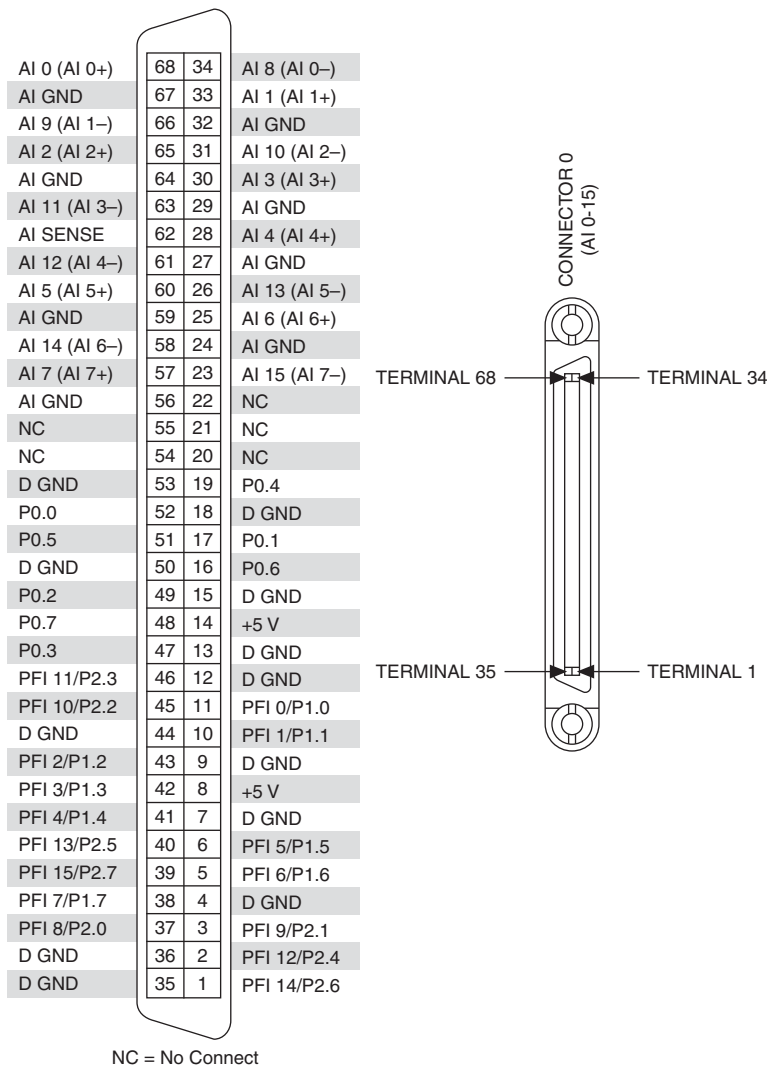
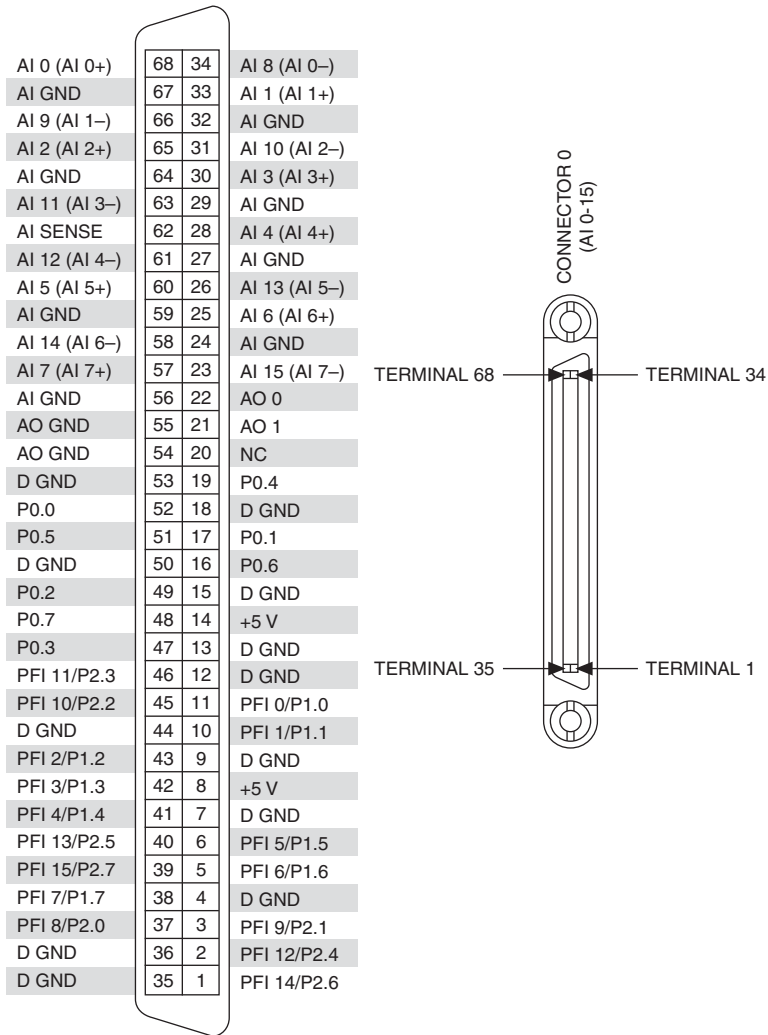
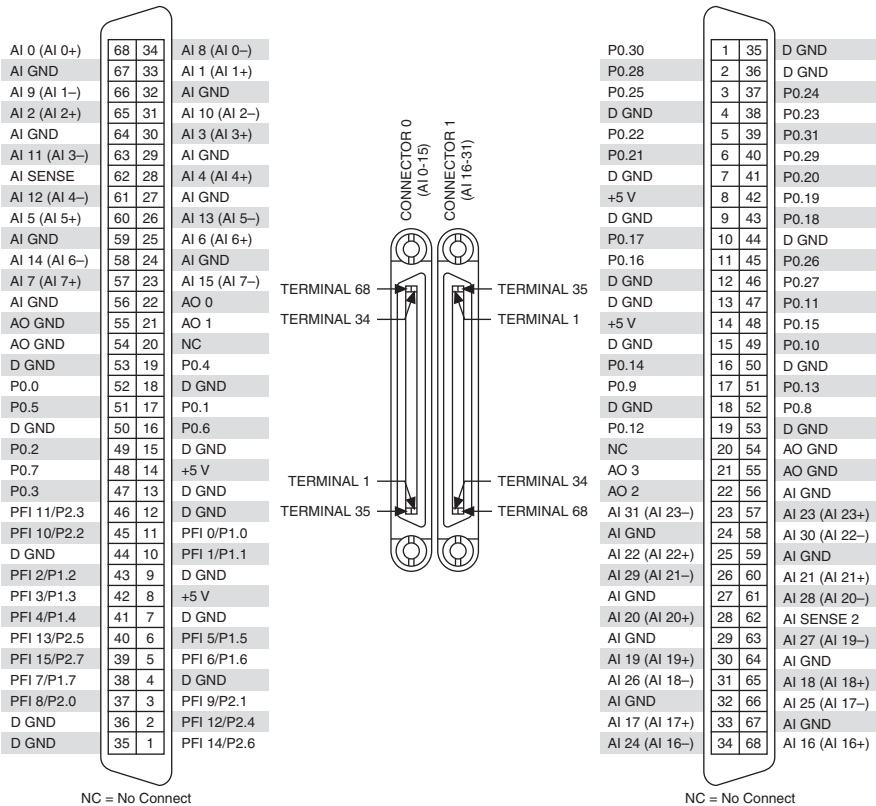


Figure 7. NI PCIe-6321 Pinout



NC = No Connect

Figure 8. NI PCIe-6323 Pinout



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